REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the pending application. The Office Action dated May 16, 2006 has been received and its contents carefully reviewed. Applicants appreciate the indication by the Examiner that claims 7-10 and 18-23 are allowable.

Claims 1-6 and 11-17 are rejected by the Examiner. Claim 3 has been amended to correct a grammatical error. No new matter has been added. Claims 1-23 are currently pending.

In the Office Action, claim 1 is rejected under 35 U.S.C. § 112 first paragraph as failing to comply with the enablement requirement. Claims 1-6 and 11-17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' Related Art (hereinafter "ARA") in view of U.S. Patent Application, Publication No. 2002/0196221 by Morita (hereinafter "Morita") and further in view of U.S. Patent Application, Publication No. 2001/0038372 by Lee (hereinafter "Lee").

The rejection of claim 1 under 35 U.S.C. § 112 first paragraph as failing to comply with the enablement requirement is respectfully traversed and reconsideration is requested.

In rejecting claim 1 under 35 U.S.C. § 112 first paragraph, the Examiner alleges that "The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention." The Examiner points particularly to "reducing the number of bits of source data, thereby generating a reduced-bit source data, wherein reducing the number of bits of includes converting an odd source data value into an even source data value." The Examiner further contends that "includes" in this context is ambiguous. Applicants respectfully disagree that the Applicants' specification is not enabling or that "includes" is ambiguous.

As to the intended meaning of "includes", the MPEP states "The transitional term "comprising", which is synonymous with "including," "containing," or "characterized by," is inclusive or open-ended and does not exclude additional, unrecited elements or method

steps." See MPEP 2111.03. Accordingly, Applicants submit that the meaning of "includes" as a transitional term as used in the claim 1 is well known and is not ambiguous.

Further, the Applicants' specification provides an example implementation of the claimed feature stating, "If the value of the 8-bit source data is an odd number in the step S1, each of the first and second converters 59A and 59B may subtract `1` from the odd data to turn the odd data into an even data (steps S2 and S3). Subsequently, each of the first and second converters 59A and 59B may divide the converted 8-bit even data by `2` and may convert the divided data into the 7-bit data, then may supply the converted 7-bit data to the lookup table 52." See Applicants' specification page 22, lines 1-6 as filed. Applicants submit that from at least this portion of the Applicants' specification, one of ordinary skill in the art would be able to make and/or use the invention as claimed.

For the reasons given above, Applicants submit that claim 1 complies fully with 35 U.S.C. § 112, first paragraph and respectfully request that the rejection to claim 1 under 35 U.S.C. § 112, first paragraph be withdrawn.

In the Office Action, claims 1-6 and 11-17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over ARA in view of Morita and further in view of Lee. Applicants respectfully traverse the rejection of independent claim 1 and request reconsideration. Applicants submit that ARA, Morita and Lee do not teach each and every element of the claims.

Claim 1 recites a method for driving a liquid crystal display having a combination of features including "reducing the number of bits of the source data, thereby generating a reduced-bit source data, wherein reducing the number of bits includes converting an odd source data value into an even source data value." The Examiner in rejecting claim 1 cites no part of ARA, Morita, or Lee as teaching at least "wherein reducing the number of bits includes converting an odd source data value into an even source data value." Applicants submit that ARA, Morita, and Lee, analyzed singly or in combination, do not teach or suggest at least this feature of the claimed invention. Accordingly, Applicants respectfully submit that claim 1, and claims 2–6 depending therefrom, are allowable over any combination of ARA, Morita, and Lee.

Claim 11 recites an apparatus for driving a liquid crystal display having a combination of features including "a modulator for comparing the reduced-bit source data of a current frame with reduced bit source data of a previous frame to modulate the source data by using a preset modulated data in accordance with a result of the comparison, wherein a bit number of the reduced-bit source data of the previous frame is the same as that of the current frame, and a bit number of the preset modulated data is more than that of the reduced-bit source data of each previous frame and current frame, and wherein the modulator replaces all of the bits of the source data with preset modulated data."

In the rejecting claim 11, the Examiner acknowledges in the Office Action that ARA and Morita "fail to teach of a method of driving a liquid crystal display wherein a bit number of the reduced-bit source data of the previous frame is the same as that of the current frame, and a bit number of the preset modulated data is more than that of the reduced-bit source data of each previous frame and current frame, and wherein the modulator replaces all of the bits of the source data with preset modulated data."

The Examiner cites Lee to cure the deficiencies of ARA and Morita. In particular, the Examiner cites FIG. 11 and paragraphs [0096]-[0102] of Lee.

Paragraphs [0100]-[0102] of Lee state the following:

> Two bits (bits of the present frame) starting from the LSB among 8-bit gray signals transmitted to the data gray signal modifier 400 are not modified, and they are input to the data gray signal converter 480. The remaining 6 bits of the present frame are input to the data gray signal converter 480 for modification and concurrently stored in predetermined addresses of the frame memory 460.
>
> Here, since the frame memory 460 stores the bit of the present frame during a single frame period and then outputs the same, 6-bit gray signals of the previous frame are output to the data gray signal converter 480.
>
> The data gray signal converter 480 receives 6-bit R gray signals of the present frame and 6-bit R gray signals of the previous frame, generates modified gray signals considering the 6-bit R gray signals of the previous and present frames, adds the generated 6-bit gray signals and the 2-bit LSB gray signals of the present frame, and outputs finally modified 8-bit gray signals G_n.

Applicants submit that Lee does not teach at least "wherein the modulator replaces all of the bits of the source data with preset modulated data" as recited in claim 11 and thus does not cure the deficiencies in the teachings of ARA and Morita. Applicants submit that ARA, Morita, and Lee, singly or in combination, do not teach or suggest at least this feature of the claimed invention. Accordingly, Applicants respectfully submit that claim 11, and claims 12-17 depending therefrom, are allowable over any combination of ARA, Morita, and Lee.

The application is in condition for allowance and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. § 1.136, and any additional fees required under 37 C.F.R. § 1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. *A duplicate copy of this sheet is enclosed.*

Respectfully submitted,

Dated: August 16, 2006

By Valerie P. Hayes Reg. No. 53,005
f/ **Rebecca G. Rudich**
Registration No. 41,786
McKENNA LONG & ALDRIDGE LLP
1900 K Street, N.W.
Washington, DC 20006
(202) 496-7500
Attorneys for Applicant

Applicants submit that Lee does not teach at least "wherein the modulator replaces all of the bits of the source data with preset modulated data" as recited in claim 11 and thus does not cure the deficiencies in the teachings of ARA and Morita. Applicants submit that ARA, Morita, and Lee, singly or in combination, do not teach or suggest at least this feature of the claimed invention. Accordingly, Applicants respectfully submit that claim 11, and claims 12-17 depending therefrom, are allowable over any combination of ARA, Morita, and Lee.

The application is in condition for allowance and early, favorable action is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. § 1.136, and any additional fees required under 37 C.F.R. § 1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. *A duplicate copy of this sheet is enclosed.*

Respectfully submitted,

Dated: August 16, 2006

By Valerie P. Hayes Reg. No. 53,005
for **Rebecca G. Rudich**
Registration No. 41,786
McKENNA LONG & ALDRIDGE LLP
1900 K Street, N.W.
Washington, DC 20006
(202) 496-7500
Attorneys for Applicant